UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,415	02/05/2002	Ji Ung Lee	MI30-068	5182

21567 7590 08/08/2006

WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,415	LEE ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *74,75,77,78,102-106,108,109,111,113,118 and 120* is/are allowed.

6)☒ Claim(s) *79,80,83-85,88,89,92-94,96,114,116,121 and 122* is/are rejected.

7)☒ Claim(s) *81,82 and 86* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 74,75,77-86,88,89,92-94,96,102-106,108,109,111,113,114,116,118 and 120-122.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed June 1, 2006, which amends claims 74, 79, 89, 93, 102, 108 and 116, cancels claims 76, 90-91, 95, 107, 110, 117 and 119, and adds claims 120-122 has been entered. Claims 74-75, 77-86, 88-89, 92-94, 96, 102-106, 108-109, 111, 113-114, 116, 118, and 120-122 are currently pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 79 is rejected under 35 U.S.C. 102(e) as being anticipated by Hofmann et al. '605.

Hofmann et al. discloses a field effect transistor fabrication method (col. 7, lines 35-50) comprising providing semiconductive material (fig. 3, 14a) including a channel region (region under gate 17a); providing a plurality of semiconductive regions (19a/b) adjacent to the channel region of the semiconductive material, wherein at least one of the semiconductor regions comprises an emitter (13a); and self-aligning a gate with the semiconductive regions after providing the semiconductive regions (col. 8, line 65 - col. 9, line 6).

4. Claims 83-85, 88-89, 92, 116 and 121 are rejected under 35 U.S.C. 102(e) as being anticipated by Itoh et al. '107.

a. Regarding claims 83-85, 88, and 121, Itoh et al. discloses a field emission device fabrication method comprising providing a thin film semiconductor material (fig. 1, 5); providing a plurality of semiconductive regions adjacent to the semiconductive material (regions of layer 5 adjacent to channel region), and wherein the providing the semiconductive region comprises providing one of the semiconductive regions comprising a plurality of emitters (fig. 1, 9; fig. 2, 9); providing a gate intermediate the semiconductive regions (fig. 1, 3), wherein providing the semiconductive regions and the gate comprise forming a field effect transistor (fig. 1); wherein the gate is provided about one of the emitters (fig. 1, 7); and wherein the plurality of emitters are electrically coupled with a single one of another of the semiconductor regions via the gate comprising a single gate electrode (fig 1, emitters 9 coupled to region 4 via channel/gate 3).

b. Regarding claims 89 and 92, Itoh et al. discloses a field emission device operational method comprising providing a plurality of semiconductive regions (fig. 1, regions of layer 5 adjacent to channel region) adjacent to a thin film semiconductive layer comprising a channel region (fig. 1, channel region of layer 5), and wherein at least one of the semiconductive regions comprises an emitter (fig. 1, 9); controlling current flow intermediate the semiconductive regions within the channel region and controlling emission of electrons from the field emitter using a gate intermediate the semiconductive

regions (fig. 1, 3; col. 6, lines 13-24, current control electrode); and configuring the gate and the semiconductor regions to form a field effect transistor (fig. 1).

c. Regarding claim 116, Itoh et al. discloses a field effect transistor fabrication method comprising providing semiconductive material including a channel region (fig. 1, channel region of layer 5); providing a source semiconductive region (4) and a drain semiconductive region (region of layer 5 with emitters 9) adjacent to the channel region of the semiconductive material; and wherein the providing the drain semiconductive region comprises providing a plurality of emitters (fig. 1, 9; fig. 2, 9); providing a gate dielectric material (fig. 1, 6) over the channel region; and providing a gate (7) over the gate dielectric material and the channel region.

5. Claims 93-94 and 96 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. '894.

Gardner et al. discloses a field effect transistor fabrication method comprising providing a thin film semiconductive layer (fig. 1A, 102; epi layer, col. 5, lines 20-26) including a channel region (fig. 1F, 118); providing a plurality of spaced semiconductive regions adjacent to the channel region of the semiconductive layer (fig. 1F, 110A & 110B); and providing a gate dielectric material over the channel region (fig. 1H, 130), providing a gate material over the gate dielectric (fig. 1I, 136), and chemical-mechanical polishing the gate dielectric and gate material to result in upper surfaces of the gate dielectric material and semiconductive regions

to be substantially elevationally coincident with an upper surface of the gate (fig. 1J).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann et al. '605 in view of Itoh et al. '107.

Hofmann et al. discloses all of the elements of the claim as set forth in paragraph 3 above, but the reference does not explicitly disclose the field effect transistor to comprise a thin film semiconductor material. Itoh et al. '107 teaches a method of forming a field effect transistor comprising an emitter, wherein the semiconductor material including a channel region comprises a thin film semiconductor layer (fig. 1, channel region of layer 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the thin film semiconductor layer of Itoh et al. in the method of fabricating a field effect transistor of Hofmann et al. One would have been motivated to do this because using a thin film semiconductor layer over an insulating substrate to form the channel region of the FET instead of using a bulk semiconductor substrate to form the channel was a conventional method of

reducing electrical noise that occurs when using the bulk semiconductor substrate, thus improving the performance of the device.

8. Claims 114 and 122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. '107 in view of Itoh et al. '595.

Itoh et al. '107 discloses all of the elements of the claims as set forth in paragraph 4 above, but the reference does not explicitly teach the emitter region to be formed by etching. Itoh et al. '595 teaches a method of forming a field emission device wherein the emitter is formed by etching (col. 1, lines 18-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the emitter of Itoh et al. '107 using the etching process of Itoh et al. '595. One would have been motivated to do this because using an etching process to form the emitter would have provided a sharp emitter tip, thus providing a large emission current and a highly reproducible structure (Itoh et al. '595, col. 1, lines 25-30).

Response to Arguments

9. Applicant's arguments, see pages 13-16, with respect to the rejection of claims 74-75, 77-78 and 113 have been fully considered and are persuasive. The rejection of claims 74-75, 77-78 and 113 has been withdrawn.

10. Applicant's arguments, see pages 16-17, with respect to the rejection of claims 79 and 80 have been considered but are moot in view of the new ground(s) of rejection as set forth above.

11. Applicant's arguments, see pages 16-17, with respect to the rejection of claims 81 and 82 have been fully considered and are persuasive. The rejection of claims 81 and 82 has been withdrawn.

12. Applicant's arguments, see page 17, with respect to the rejection of claims 83-85, 88 and 114 have been considered but are moot in view of the new ground(s) of rejection as set forth above.

13. Applicant's arguments, see pages 17-18, with respect to the rejection of claim 86 have been fully considered and are persuasive. The rejection of claim 86 has been withdrawn.

14. Applicant's arguments, see pages 19-20, with respect to the rejection of claims 89 and 92 have been considered but are moot in view of the new ground(s) of rejection as set forth above.

15. Applicant's arguments, see page 20, with respect to the rejection of claims 93, 94 and 96 have been fully considered but they are not persuasive. Applicant argues that Gardner et al. does not teach the semiconductor regions to comprise an upper surface substantially elevationally coincident with an upper surface of the gate. This argument is not persuasive because Gardner et al. distinctly teaches the upper surface of the gate (fig. 1J, 138) to be "substantially aligned with the top surface [of the semiconductor region] 104" (col. 7, lines 44-46). While oxide layer 106 is present on top of semiconductor region 104, the thickness of layer 104 is only 50 angstroms, and therefore Gardner et al. defines this to be within the limits of the relative term "substantially aligned".

16. Applicant's arguments, see pages 20-21, with respect to the rejection of claims 102-106 have been fully considered and are persuasive. The rejection of claims 102-106 has been withdrawn.

17. Applicant's arguments, see pages 21-22, with respect to the rejection of claims 108-109 and 111 have been fully considered and are persuasive. The rejection of claims 108-109 and 111 has been withdrawn.

18. Applicant's arguments, see page 22, with respect to the rejection of claim 116 have been considered but are moot in view of the new ground(s) of rejection as set forth above.

19. Applicant's arguments, see pages 22-23, with respect to the rejection of claim 118 have been fully considered and are persuasive. The rejection of claims 118 has been withdrawn.

Allowable Subject Matter

20. Claims 74-75, 77-78, 102-106, 108-109, 111, 113, 118, and 120 are allowed.

21. Claims 81-82 and 86 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven J. Fulk
Patent Examiner
Art Unit 2891

BRADLEY K. SMITH
PRIMARY EXAMINER

August 2, 2006